REMARKS/ARGUMENTS

Claims 1-42 are pending in the present patent application. Claims 1-4, 19-20, 22, 28, 33, 38 and 40 were rejected in the second office action. Reconsideration of the claims is respectfully requested.

Allowable Subject Matter

The last office action allowed claims 39, 41, and 42. The office action indicated that claims 5-14, 16-18, 21, 23-27, 29-32, and 34-37 contain allowable subject matter.

Rejections of Claims 1-4, 19, 20, 22, 28, 33, 38, and 40

Claims 1-4, 19, 20, 22, 28, 33, 38, and 40 were rejected as being anticipated by or obvious in light of U.S. Patent 5,999,015 to Cliff et al. and U.S. Patent 5,347,181 to Ashby et al.

Claim 1 of the present application recites "An integrated circuit, comprising: programmable logic circuitry; embedded processor circuitry comprising a processor; and shared I/O circuitry coupled to the embedded processor circuitry and the programmable logic circuitry that comprises a plurality of I/O pins which are accessible by the processor and the programmable logic circuitry."

1. U.S. Patent 5,999,015 to Cliff et al.

The Cliff et al. patent describes a processor 204, a programmable logic device 10, and I/O circuitry 208. "These components are coupled together by a system bus 220 and are populated on a circuit board 230 which is contained in an end-user system 240." See Col. 10, lines 47-54. (emphasis added)

Cliff et al. does not disclose programmable logic circuitry, a processor, and shared I/O circuitry coupled to the embedded processor circuitry and the programmable logic circuitry

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that comprises I/O pins which are accessible by the processor and the programmable logic circuitry, all on one integrated circuit, as recited in claim 1.

Also, the second office action noted that Cliff et al. does not disclose a "shared I/O portion comprising first I/O pins that are accessible by circuitry in the programmable logic portion and the embedded logic portion." See page 5 of the second office action.

2. **U.S. Patent 5,347,181 to Ashby et al.**

As mentioned in the response to the first office action, the ASIC cell block 16 in Ashby et al. is an application specific integrated circuit (ASIC) block. An application specific integrated circuit is not a programmable logic circuit. An ASIC is hardwired during manufacture to implement only circuit design and cannot be reprogrammed.

A programmable logic circuit, on the other hand, can be programmed and re-programmed after it has been manufactured to implement a variety of circuit designs. A programmable logic circuit has the flexibility to implement a variety of circuit designs. An ASIC does not have this flexibility. Ashby et al. does not disclose or suggest an integrated circuit with programmable logic circuitry and a processor with shared I/O circuitry per in claim 1.

It would not have been obvious to combine the Cliff patent with the Ashby patent to achieve the claimed invention. Specifically, there is no motivation or suggestion (express or implied) in Ashby to substitute ASIC block 16 with a programmable logic device to achieve the claims of the present application.

Therefore, claims 1, 19, 20, 28, 30, 33 and 40 and their dependent claims are allowable for at least the above reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

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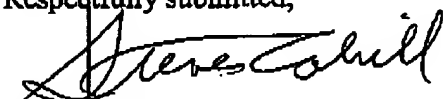
If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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